R19

Code No: 861AB

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
MCA I Semester Examinations, January - 2020
COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3hrs **Max.Marks:75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

5 ×5 Marks = 25

1.a) Explain about instruction cycle. [5]
b) What is branching? [5]
c) Write a short note on BCD complement. [5]
d) Define Memory Access time and Memory cycle time. [5]
e) Explain inter processor arbitration. [5]

PART - B

5 × 10 Marks = 50

2.a) Differentiate Computer Organization and Computer Architecture.
b) Describe the concept of Input Output interrupt. [5+5]

OR

3.a) Explain the operation of each block of digital computer.
b) State the advantages and disadvantages of the single and multiple bus organization. [5+5]

4. Illustrate different types of addressing modes with suitable examples. [10]

OR

5.a) Write and explain the micro instruction sequence for complete instruction Sequence.
b) Elaborate on control memory. [5+5]

6.a) Explain the floating point arithmetic operations in detail with diagrams.
b) Explain the operation of carry look ahead adder. [5+5]

OR

7.a) Derive an algorithm and flowchart adding and subtracting two fixed point binary numbers.
b) Explain non-restoring division algorithm with example. [5+5]

8.a) Explain memory mapped I/O.
b) Describe in detail about Virtual memory. [5+5]

OR

9.a) Explain DMA operation with a neat diagram.
b) Explain different types of priority interrupts. [5+5]

10. Explain pipelining operation. Explain how branch instructions effect pipelining operation. [10]

OR

11.a) Explain the synchronous and asynchronous data transfer.
b) Explain in detail about inter processor synchronization. [5+5]

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